Effects of Discontinuities and Technological Fluctuations on the RF Performance of BGA Packages

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Abstract

The presence of discontinuities (e.g., vias, bends…) along a uniform signal path distorts the electromagnetic (EM) field pattern, resulting in signal integrity (SI) effects especially at RF/microwave frequencies. Such effects, which also arise when geometrical and material parameters of components in chips, packages and boards unexpectedly change during the fabrication process, may lead to a degradation of the system performance, if not accounted for at the genesis of the development process. In this work, we examine the effects of discontinuities and technological fluctuations on the radio frequency (RF) performance of ball grid array (BGA) packages. For this purpose, an equivalent circuit model of the complete signal path in a BGA package was developed for frequencies up to 25GHz. The impact of multiple bends and vias on the signal quality was studied using this model. Furthermore, effects of up to 30% variation in material and geometrical parameters of each package component on its electrical characteristics and on the RF performance of the entire package were also critically investigated using the wideband package model. Based on the results of these investigations, design guidelines which can then be applied at the beginning of the development process to reduce cost and time, were deduced.

1. Introduction

As operating frequencies continuously move up the RF/microwave band, effects of discontinuities and technological fluctuations on the RF performance of BGA packages can no longer just be assumed to be negligible without prior investigations, because they cause reflections and other SI problems which may even result in the mal-functioning of the entire system. Consequently, design measures that account for these effects must be used at the beginning of the design cycle. For the development of such measures, extensive studies on the effects of discontinuities and technological fluctuations must be carried out.

Within the last decade, BGA packages have received considerable attention, mainly because of the multitude of advantages they have over other conventional packaging techniques. However, in most of the published work on electrical design of these packages, the focus has been on the extraction of parasitics using analytical, numerical and/or measurement techniques (e.g., [1] – [7]).

In this work, we used a wideband BGA package model to study the impact of discontinuities as well as geometrical and material changes on the electrical behavior of a complete signal path at RF/microwave frequencies. For the development of this model, the methodology presented in [8] was used. This methodology can be summarized as follows: In order to develop a wideband circuit model of the complete signal path (chip-to-board) in a BGA package, the boundary of each discontinuity along this path must first be defined, followed by a partitioning of the entire path into interconnecting segments and separate modeling of each of these segments. Prior to the extraction of circuit models for each segment, the modeling approach must be validated, i.e., it must be proven, that using the defined boundaries of the discontinuities, the entire signal path can be characterized using a cascade of models obtained from each interconnecting segment. To reach this goal, a 3D full-wave EM field simulation of the complete signal path must be performed within the frequency range of interest and S-parameters extracted. Each interconnecting component along this same path must also be separately simulated using the same field solver. S-parameters obtained from each of these components can then be converted to T-parameters, multiplied together and later converted again to generate S-parameters for the complete path. The modeling approach is said to be validated, if there is a very good correlation between S-parameters obtained from both sources. After the validation process, an equivalent circuit model of each segment can then be extracted. To validate these models, test structures should be designed and measured, and a good correlation must also be obtained between the measurement and simulation results. Finally, the validated circuit models obtained from each segment can then be cascaded to generate a wideband model for the entire signal path which accounts for the parasitic contribution of each interconnecting segment.

Using this methodology, a wideband BGA package model was developed in [8]. However, this model must be modified to meet the objectives of this work. The modification is presented in section two and effects of discontinuities are discussed in section three. In section four, the impact of up to 30% variations in geometrical and material parameters of each component along the signal path is presented.

2. Wideband Model for BGA Packages

In Figure 1, a cross-sectional view of the four-layered BGA package that was used for the development of the wideband circuit model is shown. The substrate is an FR4 material (ε_r=4.2, tan δ=0.007) and it consists of four metal layers, a core of 150 µm thick and two prepegs, each having a thickness of 100 µm. The outer layers (each being 27 µm thick) are used for signal routing and the inner layers (each being 35 µm thick) serve as power/ground planes. The geometry of the interconnecting segments will be presented in subsequent sections.

In order to modify the circuit model for the complete signal path developed in [8], a hybrid modeling approach was

used for each segment. A segment is defined in this work to be a geometrical discontinuity (e.g., a via) together with its the interconnecting traces, long enough to allow higher-order modes excited at the discontinuity to vanish or be considered insignificant. Lumped element models were used for each discontinuity and transmission line models for uniform interconnecting traces. Each of these models was validated by comparing measurement and simulation results. Finally, the validated models were then cascaded to generate the modified circuit model of the complete signal path, shown in Figure 2. As can be seen in Figure 3, a very good correlation was obtained between S-parameters extracted from this circuit model and those from the full-wave simulation of the complete path. It should be noted, that the main difference between the model shown in Figure 2 and that in [8] lies only in the method of extracting the equivalent circuit models for each segment. In [8], either a lumped or multi-lumped model was used for each segment, whereas in this work, a segment is represented by a combination of lumped and transmission line models.

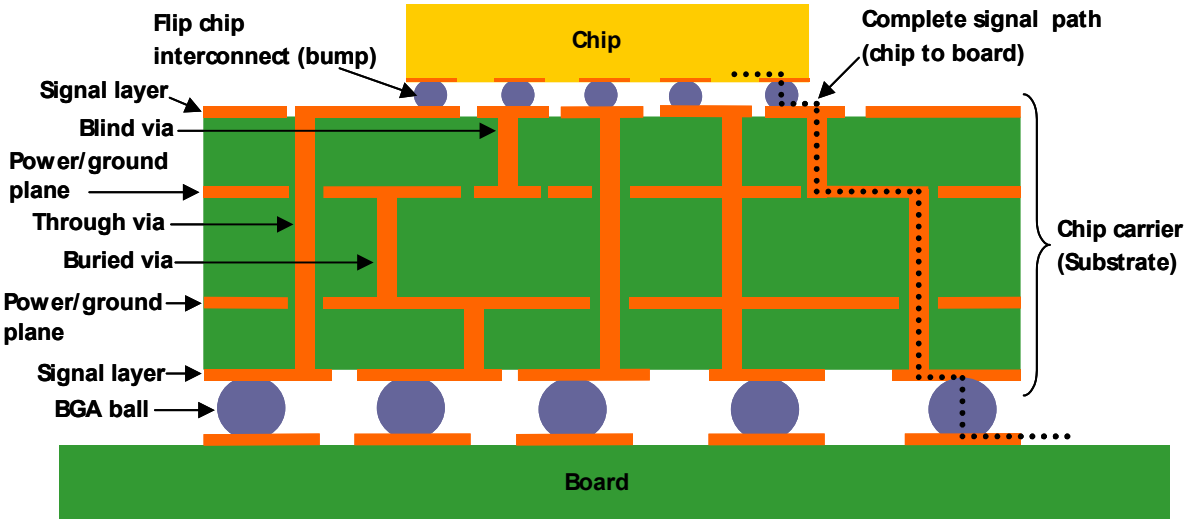

Figure 1: Schematic cross-sectional view of a BGA package [8].

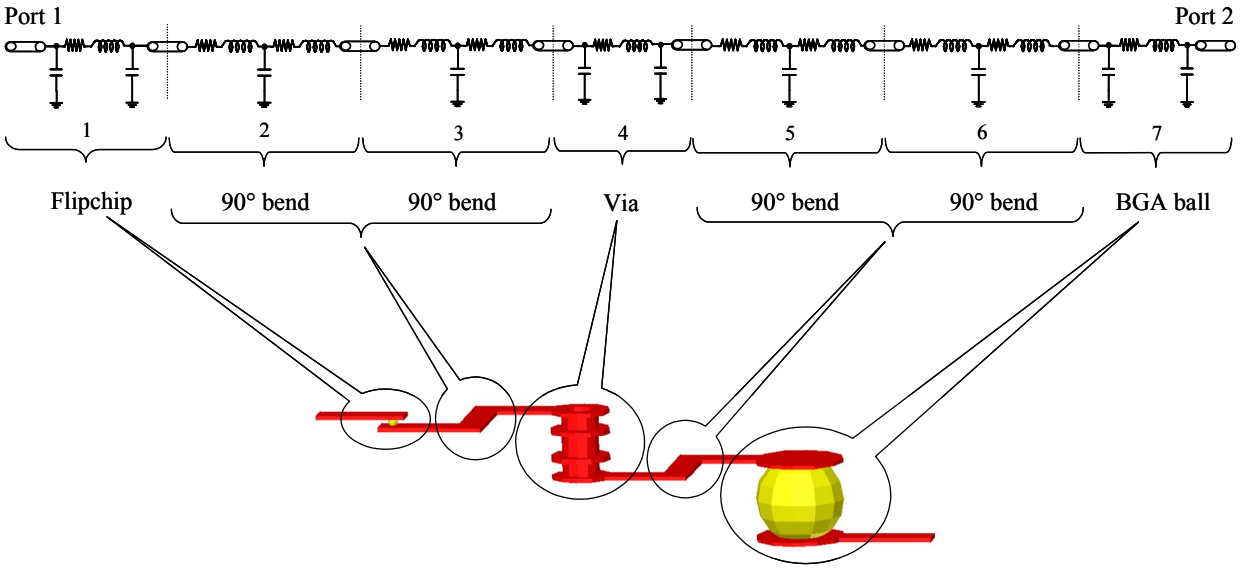

Figure 2: Equivalent circuit model of the complete signal path (chip-to-board) in a BGA package.

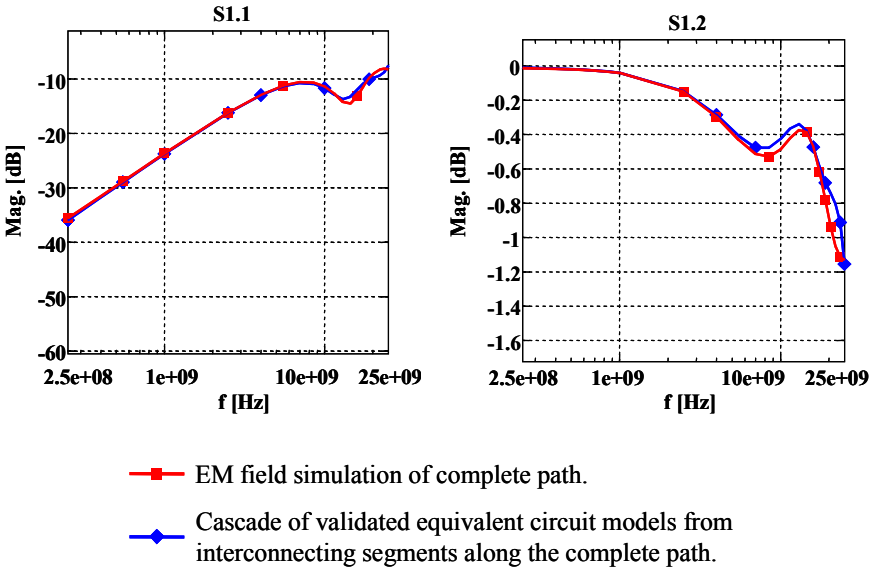

Figure 3: Comparison of S-parameters obtained from equivalent circuit model and EM field simulation of complete signal path.

3. Effects of Bends and Vias on a Signal Path

Although discontinuities have been a major subject of research for decades, most of the effort in the published work has been concentrated in studying the effects of a single discontinuity on the timing and quality of a propagating signal. In this section, we present a technique for studying the effects of multiple discontinuities (e.g., bends and vias) on the electrical behavior of a signal path in a BGA package.

Our approach involves developing an equivalent circuit model that accounts for the parasitic contribution from all interconnecting segments along the entire signal path. An example of such a model is shown in Figure 2. Using this model, the impact of each discontinuity can be studied by simply replacing its equivalent circuit model with a transmission line model that represents a uniform trace having the same length as the discontinuity. By comparing properties of the signal which propagates through the path in the presence and absence of the discontinuity, the impact of the discontinuity can easily be noticed.

For an illustration of this method, the discontinuities shown in Figure 4 and a 2.4 mm long microstrip signal path (line width, w=175 µm, line thickness, t=25 µm, substrate thickness, h=100 µm) within the substrate were considered as examples. Consequently, segments one and seven in the circuit model in Figure 2 were initially ignored. In order to investigate the effects of four bends, this circuit model was further reduced by ignoring segment 4, and transmission line models in the remaining segments were adjusted so as to achieve a total path length of 2.4mm. Values of electrical parameters of each bend were assigned to their respective components in this circuit model and S-parameters characterizing the path were then extracted. A 90° bend, for example, has an inductance (L) of approximately 15 pH, capacitance (C) of 23 fF and a resistance (R) of 6 mΩ (at 5.5 GHz). The number of bends was gradually reduced, one at a time, by replacing each equivalent circuit model of a bend with a transmission line model that represents a uniform trace having the same length as the bend. Each time a bend was removed from the path, new S-parameters were extracted. 45° and 90° bends were separately investigated. The equivalent circuit model of the signal path with no discontinuity (also shown in Figure 4) that served as the reference, was obtained by replacing equivalent circuit models of all four bends with a transmission line model of a uniform trace of equal length as the bends. S-parameters characterizing this signal path were also extracted.

To investigate the effects of vias on the signal path, only segment 4 in the circuit model in Figure 2 was used and transmission line models of the uniform interconnecting traces were extended, so as to achieve a 2.4 mm long signal path. S-parameters characterizing this path were then extracted. The through-hole via used for these investigations has the following dimensions: diameter of via pad=400 µm, diameter of via hole=200 µm, length of via=474 µm, space to ground=70 µm. For this via configuration, approximately 180 pH, 160 fF and 40 mΩ (at 5.5 GHz) were extracted for L, C and R.

Finally, a comparison was made between S-parameters characterizing the effects of the discontinuities (bends and vias) and those of the reference path. The results of this comparison are shown in Figure 5 (left and middle). Due to the presence of a 90° bend, the magnitude of S_{11} increases by approximately 4 dB from about 2.5 GHz to 20 GHz. A 45° bend on the other hand causes an approximate increase of 1 dB. As the number of bends increases, the fraction of signal reflected increases steadily with frequency. For example, four 90° bends along the path cause more than 10% of the propagating signal to be reflected at frequencies above 10 GHz. However, as can be seen in Figure 5 (left), this amount of reflection is slightly less than that caused by a single through-hole via.

From these investigations, the following guidelines were deduced: 45° bends should be used instead of 90° bends, whenever possible. Secondly, for frequencies up to 15 GHz, six 45° bends can be used along a signal path and less than 10% of the propagating signal will be reflected. Thirdly, as can be seen in Figure 5 (left and middle), the presence of any other discontinuity (e.g., a via) along a path overshadows the effects up to four bends. Consequently, if the entire signal path in a BGA package (chip-to-board) is considered, then the effects of up to four 45° bends on the magnitude of S_{11} and S_{12} of this signal path can be neglected from 100 MHz up to 25 GHz, as can be seen in Figure 5 (right).

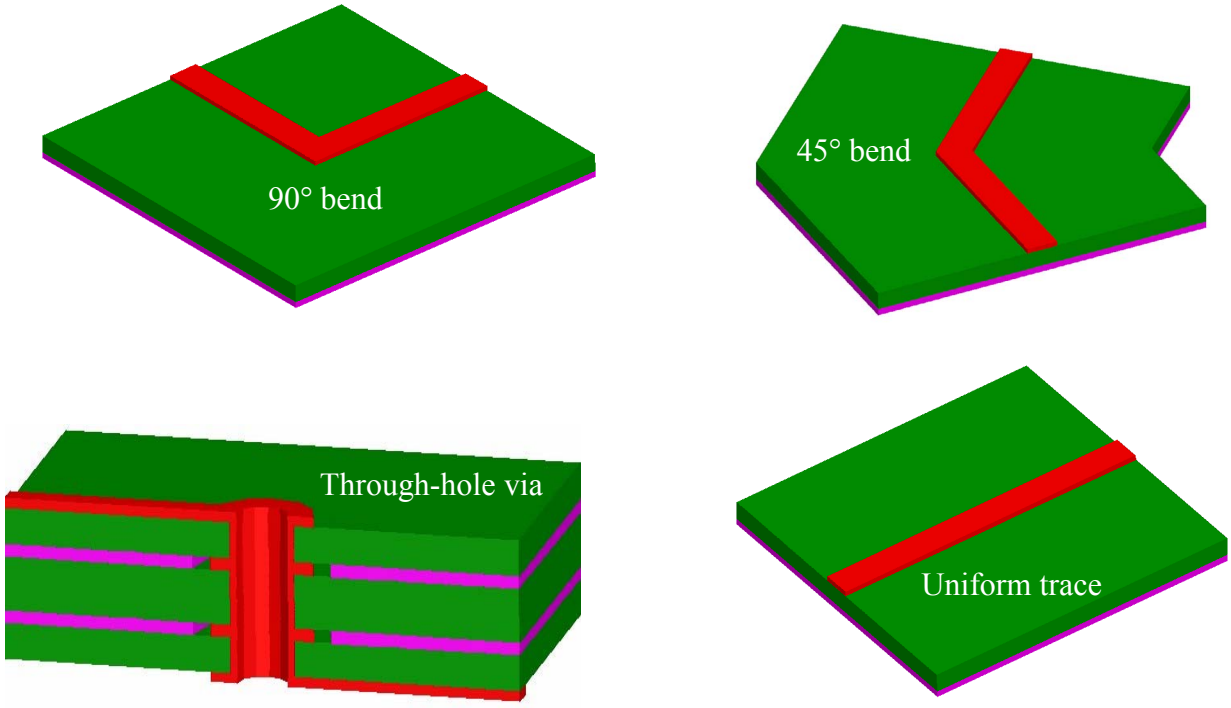

Figure 4: 3D model of a 90° bend, 45° bend, a through-hole via and a uniform microstrip trace. These structures were used to investigate the effects of discontinuities on a 2.4 mm long signal path in a BGA package.

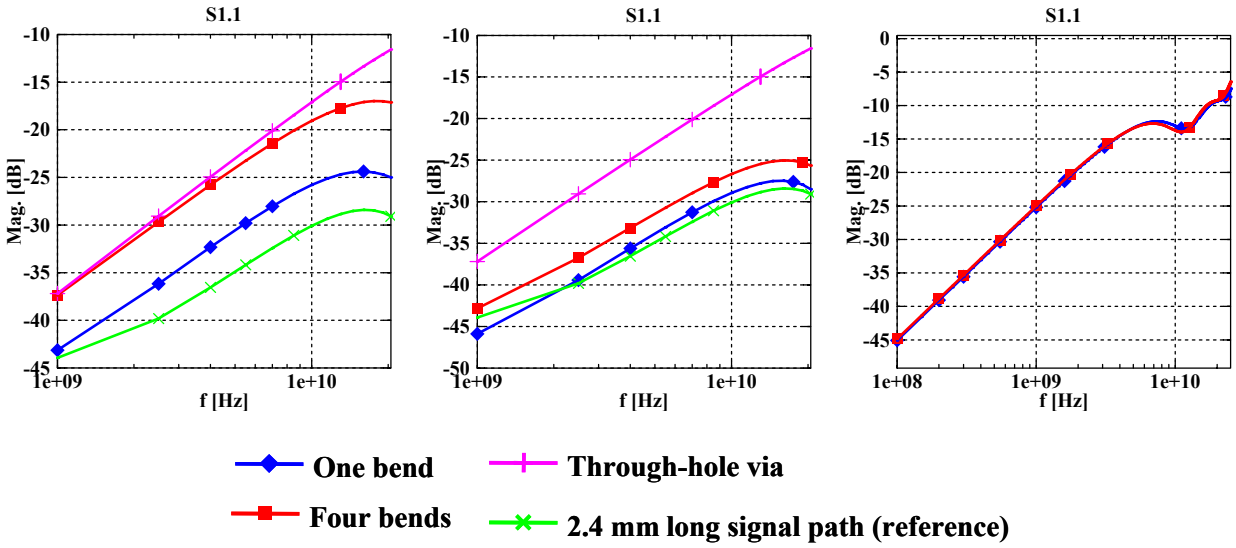

Figure 5: Effects of bends and vias on the magnitude of S_{11} of a 2.4 mm long microstrip trace (left and middle). Illustrating the negligible effects of 45° bends on the magnitude of S_{11} of the complete path (right).

4. Effects of Technological Fluctuations

When geometrical and material parameters of components fluctuate during the fabrication process, their RF characteristics also change. This may, for example, lead to unexpected impedance mismatch between interconnecting components, resulting in additional signal reflections that were not taken into consideration during the design phase. When this occurs, the normal functioning of the system can no longer be guaranteed. In order to develop design guidelines that can be used to prevent such occurrences, the impact of technological fluctuations on each package component as well as on the entire signal path must be critically investigated. To reach this goal, the following approach was used:

For each package component, a design space which defines the technological parameters of interest and the range in which they are allowed to vary was first set-up. Using standard values of these parameters, a full-wave EM simulation was performed, from which values of the required electrical parameters were extracted using an appropriate equivalent circuit model of the component under investigation. These values then served as reference. Each time a geometrical or material parameter was changed, field simulations were performed and new electrical parameter values were also extracted. These values were then compared with the reference, so as to understand the effects of the change on the electrical characteristics of the component. Since previous investigations revealed, that effects of an interaction of geometrical and/or material parameters within the defined design space can be neglected, this interaction will not be presented in this paper.

To understand the effects of technological fluctuations of each component on the RF behavior of the entire signal path, the equivalent circuit model in Figure 2 was used. Values of electrical parameters obtained from, for example, a 10% change in the diameter of a via hole, were inserted into the equivalent circuit model of the via, while the other circuit models contain the reference values. S-parameters characterizing the complete path were then extracted and compared with those obtained when all circuit parameters along the path contain only reference values. From this comparison, it will then be evident if a change in the geometrical or material parameter of the component under consideration has an impact on the S-parameters of the entire signal path.

In the following subsections, a summary of results obtained using the approach outlined above, as well as design guidelines deduced from the investigations will be presented.

4.1 Flip Chip Interconnects (Bumps)

In Figure 6, a 3D model of the flip chip configuration that was used for the sensitivity studies is shown. The geometrical parameters of interest and their standard values are: bump height=50 µm and bump diameter=60 µm. Using these values, an EM field simulation was performed. From the simulation results, approximately 0.03 nH and 25 mΩ (at 5.5 GHz) were obtained for L and R, respectively, through an optimization of the equivalent circuit model of the bump, shown in segment 1 in Figure 2.

The bump height and diameter were then varied and each time a change was made, new values of L and R were extracted. The results of these investigations revealed, that a 10% variation in the height as well as diameter of the bump causes a change of less than 5% in L and R. All fluctuations in L and R are directly proportional to changes in the bump height, but inversely proportional to the bump diameter.

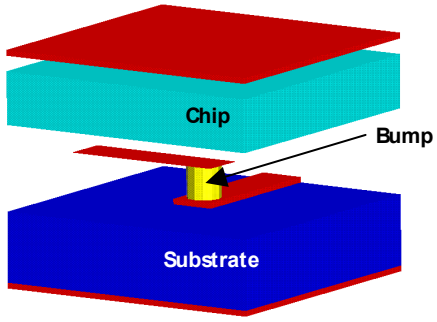

Figure 6: 3D model of a single bumped flip chip.

Since bumps are much smaller than other components along the signal, the effects of up to 30% fluctuation in their diameters and heights on the magnitude of the reflection and transmission coefficients of the S-parameters (S_{11} and S_{12}) of the entire signal path can be neglected. As can be seen in Figure 7, the curve representing the effects of a 30% change in the bump diameter lies exactly over the curve extracted when only reference values were used in the equivalent circuit model in Figure 2.

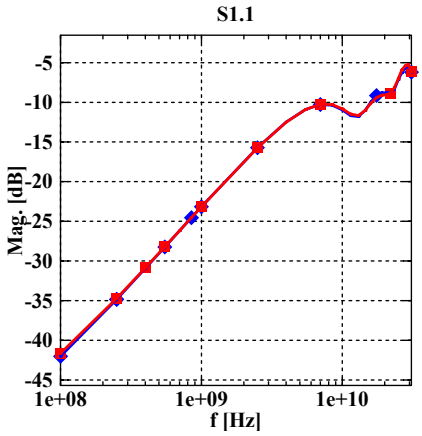

Figure 7: Comparing the magnitudes of S_{11} of the complete path, when effects of 30% variation in bump diameter are considered and when they are neglected.

4.2 Uniform Package Traces

The dimensions of the microstrip package traces given in section three were considered as standard values. Using Maxwell 2D Extractor, EM field simulations were performed each time a parameter was changed and the following results were obtained: the effects of up to 30% fluctuation in t and tan δ can be neglected, because they cause less than 5% change in Z. The most significant variation in Z was caused by fluctuations in h and w, followed by ε_r. Z changes by less

than 10% if either h, w or t fluctuates by 10% and by approximately 15% if either w or h changes by 30%. Consequently, to keep fluctuations of Z below 10%, care must be taken during the fabrication process to keep changes in w, h and ε_r below 10%.

To understand the effects of fluctuations of dominant parameters on the RF performance of the package, these parameters were separately changed from 0% to 30% and S-parameters characterizing each of these changes were extracted. The results show, that a 30% change in either h, w or ε_r cause about 3 dB change in the magnitude of S_{11} of the complete signal path. This variation in S_{11} is directly proportional to changes in w and t, and inversely proportional to changes in h. In Figure 8, the effects of a 30% variation in w on the magnitude of S_{11} is shown, as an example.

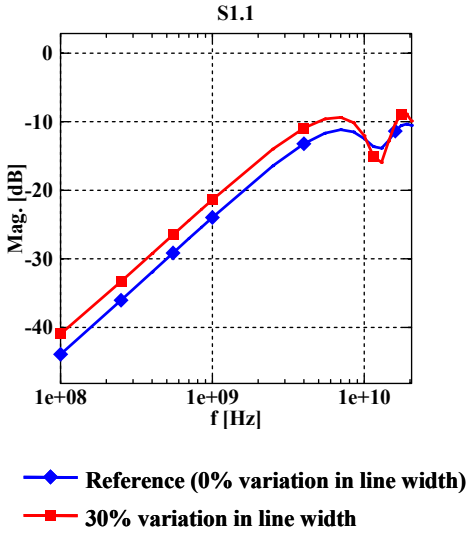

Figure 8: Comparing the magnitudes of S_{11} of the complete path, when effects of 30% variation in line width (w) are considered and when they are neglected.

4.3 Through-hole Vias

The 3D model of the through-hole via used to investigate the effects of technological fluctuations is shown in Figure 4 and the parameters of interest are presented in section 3.

The capacitance of this via is strongly influenced by ε_r, pad diameter and space to ground. A 10% change in ε_r and space to ground causes less than 10% fluctuation in C, while a 10% change in the pad diameter causes approximately 10% variation in C. C varies by approximately 10-15%, 20-25% and 25-30% if the space to ground, ε_r and pad diameter, respectively, fluctuates by 30%.

The inductance as well as capacitance of a via is highly dependent on the length of the via, which in turn depends on the dielectric thickness. But, varying the thickness of either both prepeg layers or core by 10%, causes less than 5% change in L and C. However, if prepeg and core layers simultaneously fluctuate, then both L and C will vary considerably. Such a change must be prevented, whenever possible. Fluctuations in pad diameter, space to ground as well as hole diameter also slightly affect L. For example, 30% variation in hole and pad diameters causes approximately 10% and 10-15% change in L, respectively. Changing the space to ground by 30% leads to approximately 5% fluctuation in L.

Effects of up to 30% variation in tan δ on both L and C can be neglected. This also applies to the hole displacement, if actually the interconnecting signal trace is not disconnected by such a fluctuation.

To capture the effects of fluctuations in any via parameter on the complete signal path, values of L and C resulting from a variation of the parameter in question were inserted into the equivalent circuit model of the via in segment 4 in Figure 2. In Figure 9, effects of 30% variation in the space to ground on the magnitude of S_{11} is shown as an example. At lower frequencies, the change in space to ground can be neglected, but at frequencies above 10 GHz, the impact of this change on the magnitude of S_{11} slowly becomes evident.

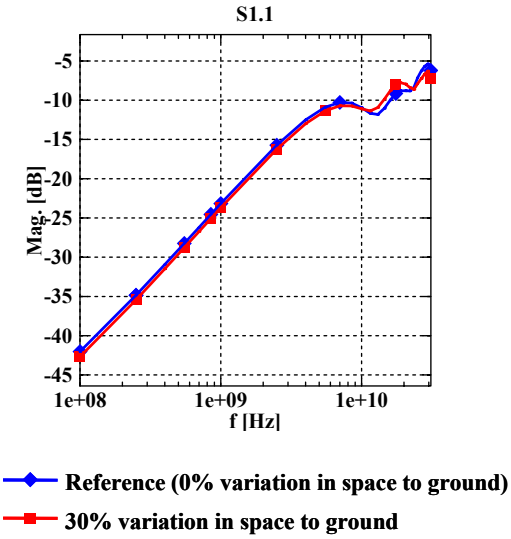

Figure 9: Comparing the magnitudes of S_{11} of the complete path, when effects of 30% variation in space to ground are considered and when they are neglected.

4.4 BGA Balls

BGA balls are the largest components along the signal path, with a diameter of 600 µm and length of 500 µm. Based on the EM field simulation of the 3D model shown in Figure 10, approximately 0.2 nH and 16 mΩ were extracted as values for L and R, respectively, using the equivalent circuit model of the ball shown in segment 7 in Figure 2.

While a 10% variation in ball height causes approximately 10% variation in L, a 10% fluctuation in the ball diameter causes slightly less variation in L as the ball height. However, if the ball diameter varies by 30%, L will vary by approximately 20%. A 30% fluctuation of ball height must be prevented whenever possible, because it causes more than 30% fluctuation in L.

Considering the complete signal path, the impact of a 30% variation in ball height on the magnitude of S_{12} becomes evident only from frequencies above 10 GHz, as can be seen in Figure 11. At 20 GHz, for example, this large variation in the ball height cause a change in approximately 1 dB in S_{12}.

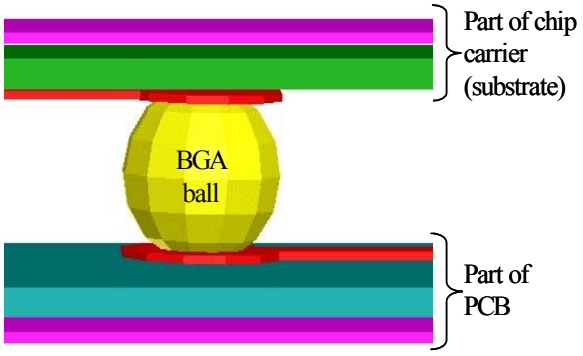

Figure 10: 3D model of a BGA ball.

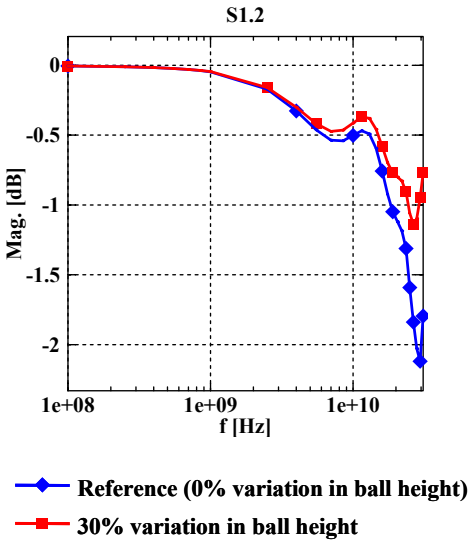

Figure 11: Comparing the magnitudes of S_{12} of the complete path, when effects of 30% variation in ball height are considered and when they are neglected.

5. Summary

In order to effectively study the effects of discontinuities as well as technological fluctuations on the RF performance of BGA packages, a wideband model that accounts for the parasitic contribution of each segment along the complete signal path (chip-to-board) was developed. Using this model, design guidelines for discontinuities were deduced. For example, it was realized that the effects of up to four 45° bends on S-parameters of the complete path can be neglected. Furthermore, with the help of this wideband model, it became evident, that large variations in electrical parameters of individual components caused by, for example, 30% fluctuation in technological parameters become insignificant when all components along the signal path are considered.

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7. References

1. Caggiano, M.F., Barkley, E., Sun, M., Kleban, J.T.,; "Electrical Modeling of the chip scale ball grid array package at radio frequencies", Elsevier Microelectronics Journal 31, 2000, Page(s) 701-709.
2. Hamano, T., Ikemoto, Y., "Electrical characterization of a 500 MHz frequency EBGA package", IEEE Transactions on Advanced Packaging Volume: 24, Issue: 4, Nov. 2001, Pages: 534 – 541.
3. Yong Kee Yeo, Iyer M.K., Youlin Qiu, Mook Seng Leong, Ban Leong Ooi, "High frequency characterization of a chip scale BGA package", Asia Pacific Microwave Conference, Volume: 3, Nov. 30 - Dec. 3, 1999, Pages: 966 – 970.
4. Caggiano, M.F., Bulumulla S., Lischner D., "RF electrical measurements of fine pitch BGA packages", 50th Electronic Components and Technology Conference, 21-24 May 2000, Pages: 449 – 453.
5. Jaeyong Jeong, Seungki Nam, Shin Y.S., Kim Y.S., Jichai Jeong, "Electrical characterization of ball grid array packages from S-parameter measurements below 500 MHz", IEEE Transactions on Advanced Packaging, Volume: 22 , Issue: 3, Aug. 1999, Pages: 343 – 347.
6. Mattei, C., Agrawal A.P., "Electrical characterization of BGA packages", 47th Electronic Components and Technology Conference, 18-21 May 1997, Pages: 1087 – 1093.
7. Solomon, D., Del Rosario E., Opiniano E., Jackson Wong, Pinello W., "Electrical characterization of metal enhanced BGA packages", 49th Electronic Components and Technology Conference, 1-4 June 1999, Pages: 848 – 852.
8. Ndip, I., Sommer, G., John, W., Reichl, H., "Methodology for Efficient Modeling of BGA Packages at RF/Microwave Frequencies", 37th International Symposium on Microelectronics (IMAPS 2004), Long Beach, CA, U.S.A, November 16-20, 2004.